HIGH VOLTAGE POSITIVE AND NEGATIVE TWO-PHASE DISCHARGE SYSTEM AND METHOD FOR CHANNEL ERASE IN FLASH MEMORY DEVICES

ABSTRACT OF THE DISCLOSURE

An erase discharge circuit in a flash memory is coupled to an array source and a p-well drive and receives first and second discharge signals. The erase discharge circuit operates during a discharge cycle in a first mode in response to the first discharge signal to couple the first node to the second node and to discharge voltages on the first and second nodes at a first rate. The erase discharge circuit operates in a second mode in response to the second discharge signal to couple the first node to the second node to discharge the voltages on the first and second nodes at a second rate.